PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10022428	12/20/2001	~~326~~ 714	726	~~2854~~ 2133	~~TABONE~~

**APPLICANTS: Matsushima Yusuke;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:
JAPAN 2000-387597 12/20/2000

PG-PUB DO NOT PUBLISH ☐ RESCIND ☐

Foreign priority claimed	☐ yes ☐ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no	NEC01P202
Verified and Acknowledged Examiners's initials		

TITLE : Master-slave-type scanning flip-flop circuit for high-speed operation with reduced load capacity of clock controller

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G
ISSUE FEE: Amount Due / Date Paid	Primary Examiner	DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAIMER	PREPARED FOR ISSUE	Application Examiner

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